REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Rejection of Claims 1-5 Under 35 USC §112, 1st Paragraph

This rejection is respectfully traversed on the grounds that electrical tests for determining whether voids have been formed are well-known to those skilled in the art. It is simply necessary to measure an electrical parameter that is affected by the presence of a void, such as voltage, current, inductance, or capacitance.

Measurement of electrical parameters such as voltage, current, and so forth is easily accomplished by those skilled in the art, by connecting two gate lines to a measuring instrument, applying a current or voltage to the probes, and reading the resulting voltage, current, inductance, or capacitance value. For example, since the trench is filled with a dielectric, the potential between the gate lines should be **zero** if no void exists. If the voltage drop value deviates from the expected value, *i.e.*, from the expected value of zero, then a void must be present.

The invention does not involves a mysterious new test for finding voids, but rather makes use of known electrical testing methods, such as measuring voltage, current, inductance, or capacitance. The uniqueness of the invention lies in setting aside a region of a **wafer**, as opposed to a cut and packed product, and carrying out the testing on a test region of the **wafer**, rather than on the finished product ***after*** the wafer has been cut and packed.

Although it is believed that skilled in the art would be familiar with the usual tests for an electrical product, including voltage, current, inductance, and capacitance testing, page 1 of the specification has been amended to explain that it is, in fact, conventional to use such tests to find voids, albeit on a finished product ***after*** cutting and packing. Because the addition to page 1, line 22 merely points out what is well-known to those skilled in the art, it is respectfully submitted that the addition does not involve "new matter."

In addition, page 3, line 12 and page 3, line 16 have been amended to more explicitly explain that the electric testing could, by way of example, involve "*measuring the potential between two gate lines 31' with a proper voltage applied thereto to obtain a value other than 1 if the void 33 exists, and a value 0 if the void 33 does not exist.*" This description follows from the well-known fact that a trench filled with dielectric should not cause a potential difference, and also does not involve "new matter."

Because the electric test can be any well-known electric test, such as measuring a potential, current, inductance, or capacitance across two gates, such tests being commonly used to test for voids *after* cutting of the wafer (although not before cutting), it is respectfully submitted that the rejections of claims 1 and 4 under 35 USC §112, 1st Paragraph is improper, and withdrawal of the rejection is respectfully requested.

2. Rejection of Claims 1-5 Under 35 USC §112, 2nd Paragraph

This rejection has been addressed by amending claim 1 to delete the recitation of "predetermined," although it is respectfully noted that "predetermined" is very commonly used in both process and non-process claims and has not (at least in the last 50 years) been considered to be a nebulous mental step. Predetermined length simply means that the length is not random or arbitrary.

In addition, claim 1 has been amended to specify that the active areas, trenches, and gate lines are formed in the test region of the wafer, while claim 5 has been amended to delete "predetermined."

Having thus overcome the grounds for rejection under 35 USC §112, 2nd Paragraph, withdrawal of the rejection is respectfully requested.

3. Rejection of Claims 1-2 Under 35 USC §102(b) in view of Admitted Prior Art on Page 1 of Applicant's Specification

This rejection is respectfully traversed on the grounds that the Applicant has not admitted that performing electric tests on a wafer is prior art. Instead, the admitted prior art specifically involves testing of a cut and packed finished semi-conductor product. As explained in lines 21-23 on page 1 of the original specification: "*Usually, the existence of the void only can be found in the electric testing, which is performed* ***after*** *the wafer is finished, cut into chips and packed. Accordingly, a waste of process is generated.*" In other words, the "admission" only involves testing that occurs after the wafer is no longer a wafer. The "admission" does not involve testing of a region of a wafer, before the wafer has been cut and packages into semiconductor devices.

The point of the invention is to test a **region** of the wafer. Such testing provides an indication of whether the entire wafer is defective, since it is likely that if voids appear in one part of the wafer, voids will appear in other parts. Therefore, the invention provides for the construction of active regions and gates on one region of the wafer, ***before any additional work is done on the wafer.*** If the wafer is defective, no further work needs to be done. This is more efficient than waiting until entire wafer is has been formed into semiconductor devices that can be individually tested.

In addition to reciting testing of a region of the wafer rather than finished products, claim 1 now recites that the active regions are **formed to have a length *longer than at least two gate lines*.** This recitation is supported by the description on page 3, lines 9-10, that ". . .*since the section of the void 33 is long, the void 33 crosses at least two gate lines 31'*. . .," and therefore does not constitute "new matter." The **admitted prior art** clearly does **not** involve such an **extended length active region**, which is useful solely for wafer testing purposes.

Because the subject matter of claims 1 and 2 is not admitted prior art, withdrawal of the rejection of claims 1 and 2 under 35 USC §102(b) is respectfully requested.

4. Rejection of Claim 5 Under 35 USC §103(a) in view of Admitted Prior Art and U.S. Patent No. 6,714,031 (Seki)

This rejection is respectfully traversed on the grounds that the Applicant has not admitted that using active areas **longer than at least two gate lines** is prior art, and on the grounds that the Seki patent also does not disclose or suggest test-region active areas that are longer than at least two gate lines. While Seki discloses formation of test circuits in "scribe regions" or cutting lines of a wafer (formation of the test circuits in the cutting regions avoids taking up useful space on the wafer, saving costs), Seki clearly does not disclose active areas longer than two gate lines, as claimed. To the contrary, the test circuits of Seki are series of transistors, which require individual active areas. Accordingly, withdrawal of the rejection of claim 5 under 35 USC §103(a) is respectfully requested.

5. Claims 3 and 4

These claims have not been rejected on prior art. It is believed that these claims are clearly directed to allowable subject matter since the prior art does not disclose or suggest, whether considered individually or in any reasonable combination, a comb-shaped gate applied to a test region of a wafer.

Having thus overcome each of the rejections made in the Official Action, withdrawal of the rejections and expedited passage of the application to issue is requested.

Respectfully submitted,

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